Amendments to the Claims:

Please amend claims 1, 4-7, 9-21, 23 and 25-29 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) A data output circuit comprising:

a first inversion unit receiving, at an input thereof, a first data signal of an operating voltage level and inverting the received first data signal to obtain, at an output thereof, a first inverted data signal;

a first voltage compensation unit coupled to the output of the first inversion unit, that compensates ~~compensating~~ for the voltage level of the first inverted data signal to obtain a first driving signal, [[if]]when a first power supply voltage of an output voltage level is different from a second power supply voltage of the operating voltage level by at least a predetermined voltage level;

a second inversion unit receiving, at an input thereof, a second data signal with the operating voltage level and inverting the received second data signal to obtain, at an output thereof, a second inverted data;

a second voltage compensation unit coupled to the output of the second inversion unit, that compensates ~~compensating~~ for the voltage level of the second inverted data signal to obtain a second driving signal, [[if]]when the levels of the first and second power supply voltages are different by at least a predetermined voltage level; and

a driver unit receiving the first and second driving signals and outputting an output data signal of a logic level that is opposite the logic levels of the first and second driving signals.

2. (original) The data output circuit of claim 1, wherein the first inversion unit forms an inverter comprising a first PMOS transistor and a first NMOS transistor serially connected between the first power supply voltage and a first ground voltage of the output voltage level, and wherein the first data signal is applied to a gate of the first PMOS transistor and a gate of the first NMOS transistor.

3. (original) The data output circuit of claim 1, wherein the second inversion unit forms an inverter comprising a second PMOS transistor and a second NMOS transistor serially

connected between the first power supply voltage and a first ground voltage of the output voltage level, and wherein the second data signal is applied to a gate of the second PMOS transistor and a gate of the second NMOS transistor.

4. (currently amended) The data output circuit of claim 1, wherein the first voltage compensation unit comprises:

a first compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage; and

a second compensation PMOS transistor, a source of which is connected to the drain of the first compensation PMOS transistor, a gate of which is subjected to the first data signal, and a drain of which is connected to a connection node between the first PMOS transistor and the first NMOS transistor.

5. (currently amended) The data output circuit of claim 4, wherein the first voltage compensation unit compensates for the voltage level of the first inverted data signal [[if]]when the first and second power supply voltages are different by at least a threshold voltage level of the first compensation PMOS transistor.

6. (currently amended) The data output circuit of claim 1, wherein the second voltage compensation unit comprises:

a third compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage; and

a fourth compensation PMOS transistor, a source of which is connected to the drain of the third compensation PMOS transistor, a gate of which is subjected to the second data signal, and a drain of which is connected to a connection node between the second PMOS transistor and the second NMOS transistor.

7. (currently amended) The data output circuit of claim 6, wherein the second voltage compensation unit compensates for the voltage level of the second inverted data signal [[if]]when the first and second power supply voltages are different by at least a threshold voltage level of the third compensation PMOS transistor.

8. (original) The data output circuit of claim 1, wherein the first and second data signals have the same level.

9. (currently amended) The data output circuit of claim 1, wherein the first voltage compensation unit comprises:

a first compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to a first drop voltage;

a second compensation PMOS transistor, a source of which is connected to the drain of the first compensation PMOS transistor, a gate of which is subjected to the first data signal, and a drain of which is connected to a connection node between the first PMOS transistor and the first NMOS transistor;

first through N-th load PMOS transistors serially connected to the first power supply voltage; and

a first load NMOS transistor connected between the N-th load PMOS transistor and a second ground voltage, a drain of which generates the first drop voltage and a gate and a source of which are connected to each other.

10. (currently amended) The data output circuit of claim 9, wherein the first voltage compensation unit compensates for the voltage level of the first inverted data signal [[if]]when the second power supply voltage and the first drop voltage are different by at least the threshold voltage level of the first compensation PMOS transistor, and the level of the first drop voltage is determined according to the number of first through N-th load PMOS transistors.

11. (currently amended) The data output circuit of claim 1, wherein the second voltage compensation unit comprises:

a third compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to a second drop voltage;

a fourth compensation PMOS transistor, a source of which is connected to the drain of the third compensation PMOS transistor, a gate of which is subjected to the second data signal, and a drain of which is connected to a connection node between the second PMOS transistor and the second NMOS transistor;

(N+1)th through M-th load PMOS transistors serially connected to the first power supply voltage; and

a second load NMOS transistor connected between the M-th load PMOS transistor and a second ground voltage, a drain of which generates the second drop voltage and a gate and a source of which are connected to each other.

12. (currently amended) The data output circuit of claim 11, wherein the second voltage compensation unit compensates for the voltage level of the second inverted data signal [[if]]when the second power supply voltage and the second drop voltage are different by at least the threshold voltage level of the third compensation PMOS transistor, and the level of the second drop voltage is determined according to the number of (N+1)th through M-th load PMOS transistors.

13. (currently amended) A data output circuit comprising:

a first inversion unit receiving, at an input thereof, a first data signal of an operating voltage level and inverting the received first data signal to obtain, at an output thereof, a first inverted data signal, [[if]]when an output voltage level of a first power supply voltage is equal to an operating voltage level of a second power supply voltage;

a first voltage compensation unit coupled to the output of the first inversion unit, that compensates ~~compensating~~ for the voltage level of the first inverted data signal to obtain a first driving signal,[[if]]when the first power supply voltage of the output voltage level is different from the second power supply voltage of the operating voltage level is ~~the levels of the first and second power supply voltages are~~ different by at least a predetermined voltage level;

a second inversion unit receiving, at an input thereof, a second data signal of the operating voltage level and inverting the received second data signal to obtain, at an output thereof, a second inverted data signal,[[if]]when the levels of the first and second power supply voltages are the same;

a second voltage compensation unit coupled to the output of the second inversion unit, that compensates ~~compensating~~ for the voltage level of the second inverted data signal to obtain a second driving signal,[[if]]when the levels of the first and second power supply voltages are different by at least a predetermined voltage level; and

a driver unit receiving the first and second driving signals and outputting an output data signal of a logic level that is opposite the logic levels of the first and second driving signals.

14. (currently amended) The data output circuit of claim 13, wherein the first inversion unit comprises:

a first inversion PMOS transistor, a source of which is connected to the first power supply voltage and a gate of which is subjected to a first control voltage;

a second inversion PMOS transistor, a source of which is connected to the drain of the first inversion PMOS transistor, a gate of which is subjected to the first data signal, and a drain of which generates the first inverted data signal;

a first inversion NMOS transistor, a drain of which is connected to the drain of the second inversion PMOS transistor, a gate of which is subjected to the first data signal, and a source of which is connected to a first ground voltage; and

a first control voltage generation unit generating the first control voltage to have a first logic level,[[if]]when the levels of the first and second power supply voltages are the same, and generating the first control voltage to have a second logic level,[[if]]when the level of the first power supply voltage is less than that of the second power supply voltage by a predetermined voltage level.

15. (currently amended) The data output circuit of claim 14, wherein the first control voltage generation unit comprises:

a first control PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage;

first through N-th load PMOS transistors serially connected to the first control PMOS transistor; and

a first control NMOS transistor connected between the N-th load PMOS transistor and a second ground voltage, a drain of which generates the first control voltage and a gate and a source of which are connected to each other.

16. (currently amended) The data output circuit of claim 13, wherein the first voltage compensation unit comprises:

a first compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage; and

a second compensation PMOS transistor, a source of which is connected to the drain of the first compensation PMOS transistor, a gate of which is subjected to the first data signal, and a drain of which is connected to a connection node between the second inversion PMOS transistor and the first inversion NMOS transistor.

17. (currently amended) The data output circuit of claim 16, wherein the first voltage compensation unit compensates for the voltage level of the first inverted data signal [[if]]when

the first and second power supply voltages are different by at least a threshold voltage level of the first compensation PMOS transistor.

18. (currently amended) The data output circuit of claim 13, wherein the second inversion unit comprises:

a third inversion PMOS transistor, a source of which is connected to the first power supply voltage and a gate of which is subjected to a second control voltage;

a fourth inversion PMOS transistor, a source of which is connected to the drain of the third inversion PMOS transistor, a gate of which is subjected to the second data signal, and a drain of which generates the second inverted data signal;

a second inversion NMOS transistor, a drain of which is connected to the drain of the fourth inversion PMOS transistor, a gate of which is subjected to the second data signal, and a source of which is connected to a first ground voltage; and

a second control voltage generation unit generating the second control voltage to have a first logic level,[[if]]when the levels of the first and second power supply voltages are the same, and generating the second control voltage to have a second logic level,[[if]]when the level of the first power supply voltage is less than that of the second power supply voltage by a predetermined voltage level.

19. (currently amended) The data output circuit of claim 18, wherein the second control voltage generation unit comprises:

a second control PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage;

(N+1)th through M load PMOS transistors serially connected to the second control PMOS transistor; and

a second control NMOS transistor connected between the M-th load PMOS transistor and a second ground voltage, a drain of which generates the second control voltage and a gate and source of which are connected to each other.

20. (currently amended) The data output circuit of claim 13, wherein the second voltage compensation unit comprises:

a third compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage; and

a fourth compensation PMOS transistor, a source of which is connected to the drain of the third compensation PMOS transistor, a gate of which is subjected to the second data signal, and a drain of which is connected to a connection node between the fourth inversion PMOS transistor and the second inversion NMOS transistor.

21. (currently amended) The data output circuit of claim 20, wherein the second voltage compensation unit compensates for the voltage level of the second inverted data signal [[if]]when the first and second power supply voltages are different by at least a threshold voltage level of the third compensation PMOS transistor.

22. (original) The data output circuit of claim 13, wherein the first and second data signals have the same level.

23. (currently amended) A data output circuit comprising:

a first inversion unit receiving a first data signal of an operating voltage level and inverting the received first data signal to obtain a first inverted data signal,[[if]]when an output voltage level of a first power supply voltage is equal to an operating voltage level of a second power supply voltage;

a first voltage compensation unit compensating for the voltage level of the first inverted data signal to obtain a first driving signal,[[if]]when the levels of the first and second power supply voltages are different by at least a predetermined voltage level;

a first control unit generating a first control signal for controlling the operation of the first voltage compensation unit [[if]]when the levels of the first and second power supply voltages are the same and generating a second control signal for controlling the operation of the first inversion unit [[if]]when the levels of the first and second power supply voltages are different by at least a predetermined voltage level;

a second inversion unit receiving a second data signal of an operating voltage level and inverting the received second data signal to obtain a second inverted data signal,[[if]]when the levels of the first and second power supply voltages are the same;

a second voltage compensation unit compensating for the voltage level of the second inverted data signal to obtain a second driving signal,[[if]]when the levels of the first and second power supply voltages are different by at least a predetermined voltage level;

a second control unit generating a third control signal for controlling the operation of the second voltage compensation unit [[if]]when the levels of the first and second power supply

voltages are the same and generating a fourth control signal for controlling the operation of the second inversion unit [[if]]when the levels of the first and second power supply voltages are different by at least a predetermined voltage level; and

a driver unit receiving the first and second driving signals and outputting an output data signal at a logic level that is opposite to the logic levels of the first and second driving signals.

24. (original) The data output circuit of claim 23, wherein the first inversion unit comprises:

a first inversion PMOS transistor, a source of which is connected to the first power supply voltage and a gate of which is subjected to the second control signal;

a second inversion PMOS transistor, a source of which is connected to the drain of the first inversion PMOS transistor, a gate of which is subjected to the first data signal, and a drain of which generates the first inverted data signal; and

a first inversion NMOS transistor, a drain of which is connected to the drain of the second inversion PMOS transistor, a gate of which is subjected to the first data signal, and a source of which is connected to a first ground voltage.

25. (currently amended) The data output circuit of claim [[14]]23, wherein the first control unit comprises:

a first control PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage;

a first control NMOS transistor, a drain of which is connected to the drain of the first control PMOS transistor, and a gate and source of which are connected to a second ground voltage;

a first inverter connected to a connection node between the first control PMOS transistor and the first control NMOS transistor, generating the first control signal; and.

a second inverter connected to the first inverter, generating the second control signal.

26. (currently amended) The data output circuit of claim 23, wherein the first voltage compensation unit comprises:

a first compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first control signal; and

a second compensation PMOS transistor, a source of which is connected to the drain of the first compensation PMOS transistor, a gate of which is subjected to the first data signal, and a

drain of which is connected to a connection node between the second inversion PMOS transistor and the first inversion NMOS transistor.

27. (currently amended) The data output circuit of claim 23, wherein the second inversion unit comprises:

a third inversion PMOS transistor, a source of which is connected to the first power supply voltage and a gate of which is subjected to a fourth control signal;

a fourth inversion PMOS transistor, a source of which is connected to the drain of the third inversion PMOS transistor, a gate of which is subjected to the second data signal, and a drain of which generates the second inverted data signal; and

a second inversion NMOS transistor, a drain of which is connected to the drain of the fourth inversion PMOS transistor, a gate of which is subjected to the second data signal, and a source of which is connected to a first ground voltage.

28. (currently amended) The data output circuit of claim 23, wherein the second control unit comprises:

a second control PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the first power supply voltage;

a second control NMOS transistor, a drain of which is connected to the drain of the second control PMOS transistor, and a gate and source of which are connected to a second ground voltage;

a third inverter connected to a connection node between the second control PMOS transistor and the second control NMOS transistor, generating the third control signal; and

a fourth inverter connected to the third inverter, generating the fourth control signal.

29. (currently amended) The data output circuit of claim 23, wherein the second voltage compensation unit comprises:

a third compensation PMOS transistor, a source of which is connected to the second power supply voltage and a gate of which is subjected to the third control signal; and

a fourth compensation PMOS transistor, a source of which is connected to the drain of the first compensation PMOS transistor, a gate of which is subjected to the second data signal, and a drain of which is connected to a connection node between the fourth inversion PMOS transistor and the second inversion NMOS transistor.

30. (original) The data output circuit of claim 23, wherein the first and second data signals have the same level.